Data Sheet | August 1, 2008 | FN4592.2

Radiation Hardened Quad Differential Line Receiver

Intersil's Satellite Applications Flow™ (SAF) devices are fully tested and guaranteed to 100kRAD total dose. These QML Class T devices are processed to a standard flow intended to meet the cost and shorter lead-time needs of large volume satellite manufacturers, while maintaining a high level of reliability.

The Intersil HS-26C32RH-T is a Quad Differential Line Receiver designed for digital data transmission over balanced lines and meets the requirements of EIA Standard RS-422. Radiation Hardened CMOS processing assures low power consumption, high speed, and reliable operation in the most severe radiation environments.

The HS-26C32RH-T has an input sensitivity of 200mV (typ). over the common mode input voltage range of ±7V. The receivers are also equipped with input fail safe circuitry, which causes the outputs to go to a logic "1" when the inputs are open. Enable and Disable functions are common to all four receivers.

Specifications

Specifications for Rad Hard QML devices are controlled by the Defense Supply Center in Columbus (DSCC). The SMD numbers listed below must be used when ordering.

Detailed Electrical Specifications for the HS-26C32RH-T are contained in SMD 5962-95689. A "hot-link" is provided from our website for downloading**.**
http://www.intersil.com/military/

Intersil's Quality Management Plan (QM Plan), listing all Class T screening operations, is also available on our website.
http://rel.intersil.com/reports/search.php

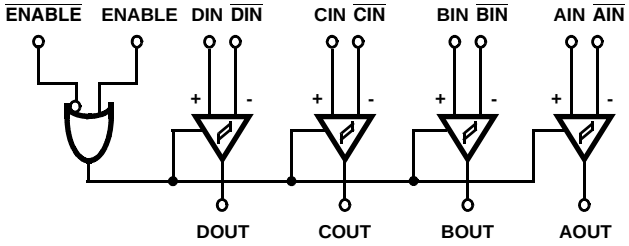
Features

- QML Class T, Per MIL-PRF-38535
- Radiation Performance
  - Gamma Dose . . . . . 1 x 10^5 RAD(Si)
  - SEU and SEL . . . . . Immune to 100MeV/mg/cm^2
- EIA RS-422 Compatible Inputs
- CMOS Compatible Enable Inputs
- Input Fail Safe Circuitry
- High Impedance Inputs when Disabled or Powered Down
- Low Power Dissipation 138mW Standby (Max)
- Single 5V Supply
- Full -55°C to +125°C Military Temperature Range

Applications

- Line Receiver for MIL-STD-1553 Serial Data Bus

Functional Diagram



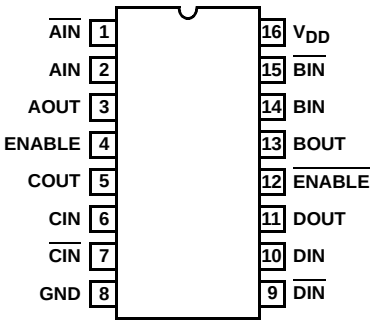
Ordering Information

ORDERING NUMBER	INTERNAL MKT. NUMBER	PART MARKING	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
5962R9568901TEC	HS1-26C32RH-T	Q 5962R95 68901TEC	-55 to +125	16 Ld SBDIP	D16.3
HS1-26C32RH/PROTO	HS1-26C32RH/PROTO	HS1- 26C32RH /PROTO	-55 to +125	16 Ld SBDIP	D16.3
5962R9568901TXC	HS9-26C32RH-T	Q 5962R95 68901TXC	-55 to +125	16 Ld FLATPACK	K16.A
HS9-26C32RH/PROTO	HS9-26C32RH/PROTO	HS9- 26C32RH /PROTO	-55 to +125	16 Ld FLATPACK	K16.A

NOTE: Minimum order quantity for -T is 150 units through distribution, or 450 units direct.

Pinouts

HS1-26C32RH-T
(16 LD SBDIP, CDIP2-T16)
TOP VIEW



HS9-26C32RH-T
(16 LD FLATPACK, CDFP4-F16)
TOP VIEW

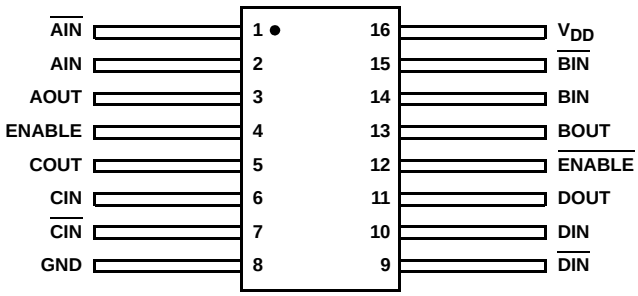


TABLE 1. TRUTH TABLE

DEVICE POWER ON/OFF	INPUTS			OUTPUT
	ENABLE	$\overline{\text{ENABLE}}$	INPUT	OUT
ON	0	1	X	HI-Z
ON	1	X	VID ≥ VTH (Max)	1
ON	1	X	VID ≤ VTH (Min)	0
ON	X	0	VID ≥ VTH (Max)	1
ON	X	0	VID ≤ VTH (Min)	0
ON	1	X	Open	1
ON	X	0	Open	1

Die Characteristics

DIE DIMENSIONS:

2140µm x 3290µm x 533µm ±25.4µm
(85 x 130 x 21mils ±1mil)

METALLIZATION:

M1: Mo/Tiw
Thickness: 5800Å
M2: Al/Si/Cu
Thickness: 10kÅ ±1kÅ

SUBSTRATE POTENTIAL:

Internally connected to V_{DD}. May be left floating.

BACKSIDE FINISH:

Silicon

PASSIVATION:

Type: SiO_2
Thickness: 8kÅ ±1kÅ

WORST CASE CURRENT DENSITY:

< 2.0e5 A/cm^2

TRANSISTOR COUNT:

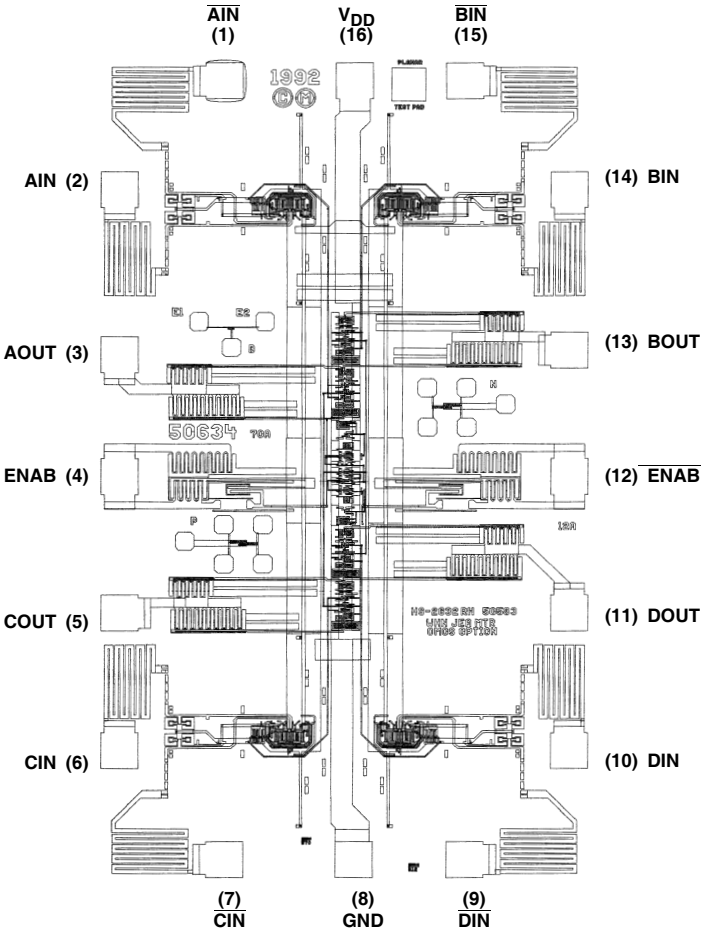
315

PROCESS:

Radiation Hardened CMOS, AVLSI

Metallization Mask Layout

HS-26C32RH



All Intersil U.S. products are manufactured, assembled and tested utilizing ISO9000 quality systems.
Intersil Corporation's quality certifications can be viewed at www.intersil.com/design/quality